What is claimed is:

1. A controller monitor circuit in a memory device, the circuit comprising:
a program memory that stores a program/erase routine;
a microcontroller circuit coupled to a selected clock signal and the program memory, the microcontroller circuit generating state machine data signals in response to the selected clock signal and the program/erase routine;
a memory array, coupled to the microcontroller circuit, for storing array data; and
an output circuit coupled to the memory array and the microcontroller for multiplexing between state machine data signals and the array data in response to the program/erase routine.

2. The circuit of claim 1 and further including a test mode decoder circuit that selects controller monitor circuit configurations and generates test mode signals.

3. The circuit of claim 2 wherein the test mode decoder circuit operates in response to address and memory device control signal inputs.

4. The circuit of claim 1 and further including a clock generation circuit that selects between an internal clock signal and an external clock signal to generate the selected clock signal.

5. The circuit of claim 4 and further including an internal clock oscillator that generates the internal clock signal.

6. The circuit of claim 1 wherein the selected clock signal comprises a plurality of clock phases.

7. The circuit of claim 1 wherein the selected clock signal has a frequency that is variable down to 0 Hz.

8. The circuit of claim 1 and further including a program/erase initiation circuit, coupled to the microcontroller, that generates control signals to initiate program or erase operations.

9. The circuit of claim 8 wherein the microcontroller includes a program counter that is adapted to be loaded with a program memory start address indicating a location in the program memory that stores an initial address of the program/erase routine.

10. A controller monitor circuit in a memory device, the circuit comprising:

a clock signal switching circuit for switching between an external clock signal and an internal clock signal to generate a selected clock signal;

a phase generation circuit for generating a plurality of clock phases from the selected clock signal;

a microcontroller circuit coupled to the plurality of clock phases, the microcontroller circuit generating state machine data signals and having a read only memory that stores program/erase routines at a predetermined address;

a flash memory array, coupled to the microcontroller circuit, for storing array data; and

an output circuit for multiplexing between at least the state machine data signals and the array data and outputting results of the multiplexing.

11. The circuit of claim 10 and further including a test mode decoder circuit coupled to the microcontroller circuit and the output circuit, the test mode decoder circuit generating test signals to set-up the controller monitor circuit and enable the output circuit to multiplex between the status signals, the state machine data signals, and the array data.

12. The circuit of claim 10 wherein the state machine data includes a read only memory address and a status of the microcontroller circuit.

13. The circuit of claim 10 wherein the microcontroller circuit comprises:

a program counter, coupled to the read only memory, for generating read only memory addresses;

an instruction decoder, coupled to the read only memory and the program counter, for accessing and interpreting the instructions from the read only memory in response to the program counter and incrementing the program counter;

a register circuit, coupled to the instruction decoder, for storing data generated from the instruction decoder and feedback signals from the flash memory array that indicate status of a memory operation; and

a start address memory, coupled to the program counter, for storing read only memory addresses indicating a location for the program/erase routines.

14. A controller monitor circuit in a memory device, the circuit comprising:

a clock signal switching circuit for switching between an external clock signal and an internal clock signal to generate a selected clock signal;

a phase generation circuit for generating a plurality of clock phases from the selected clock signal;

a microcontroller circuit coupled to the plurality of clock phases, the microcontroller circuit generating state machine data signals and having a read only memory that stores a plurality of program/erase routines, each routine at a predetermined start address;

a flash memory array, coupled to the microcontroller circuit, for storing array data;

a suspend resume controller circuit that generates memory device status data in response to memory operation interrupt and resume signals;

a state machine monitor circuit having inputs coupled to the suspend resume controller circuit and the microcontroller, the state machine monitor circuit generating a write state machine output signal in response to a multiplexing

operation between the memory device status data and the state machine data signals;

a test mode decoder circuit that generates test signals; and

an output circuit, coupled to the test mode decoder circuit, for generating an output signal in response to a multiplexing operation between the write state machine output signal and the array data, the multiplexing operation controlled by the test signals.

15. A method for debugging a memory device having a memory array and a read only memory-based microcontroller, the method comprising:

selecting test mode monitor configuration;

selecting a clock configuration;

initiating one of a program or erase operation that is executed in response to the clock configuration; and

reading debug signals on output pads of the memory device.

16. The method of claim 15 wherein initiating the program or erase operation is in response to a chip enable signal, a write enable signal, and at least one data signal.

17. The method of claim 15 wherein selecting a clock configuration further includes selecting between an external clock signal and an internal clock signal in response to the test mode monitor configuration.

18. The method of claim 17 and further including:

generating a plurality of phased clock signals from the selected clock signal; and

varying a frequency of the selected clock signal if the selected clock signal is the external clock signal.

19. A method for debugging a memory device having a memory array and a read only memory-based microcontroller, the method comprising:

initiating a first test/debug mode of a plurality of test/debug modes;

applying commands to the memory device to initiate an operation to be debugged;

generating actuator signals to the memory array to initiate memory operations in response to the operation to be debugged; and

outputting read only memory addresses, microcontroller status data, and memory array operation status data generated by the operation to be debugged.

20. The method of claim 19 wherein the operation to be debugged is a program operation.

21. The method of claim 19 wherein the operation to be debugged is an erase operation.

22. The method of claim 19 wherein the read only addresses, microcontroller status data, and memory array operation status data are output in response to multiplexing operations.

23. The method of claim 19 and further including the memory array providing feedback signals on the memory operations to the microcontroller.

24. A memory device comprising:

a memory array that stores data; and

a microcontroller monitor circuit comprising:

a switchable clock input that selects an internal clock signal in a normal mode and an external clock signal in a test/debug mode, the external clock signal having a frequency that is variable; and

a microcontroller coupled to the memory array and the switchable clock input, the microcontroller having a read only memory and outputting state machine status data in the debug mode.

25. The memory device of claim 24 wherein the memory device is a flash memory device based on a NAND architecture.

26. The memory device of claim 24 wherein the memory device is a flash memory device based on a NOR architecture.

27. The memory device of claim 24 wherein the microcontroller is further adapted to output read only memory addresses associated with the debug mode.

28. A memory device comprising:
a memory array that stores array data; and
a microcontroller monitor circuit comprising:
a switchable clock input that selects an internal clock signal in a normal mode and an external clock signal in a test/debug mode, the external clock signal having a frequency that is variable;
a microcontroller coupled to the memory array and the switchable clock input, the microcontroller having a read only memory and outputting state machine status data and read only memory addresses in the debug mode; and
a plurality of multiplexing circuits that switch between the state machine status data, the read only memory addresses, and the array data for output from the microcontroller monitor circuit.

29. An electronic system comprising:
a controller that controls the operation of the electronic system; and
a memory device coupled to the controller, the memory device comprising:
a memory array that stores data; and
a microcontroller monitor circuit comprising:
a switchable clock input that selects an internal clock signal in a normal mode and an external clock signal in a test/debug

mode, the external clock signal having a frequency that is variable; and

a microcontroller coupled to the memory array and the switchable clock input, the microcontroller having a read only memory and outputting state machine status data in the debug mode.